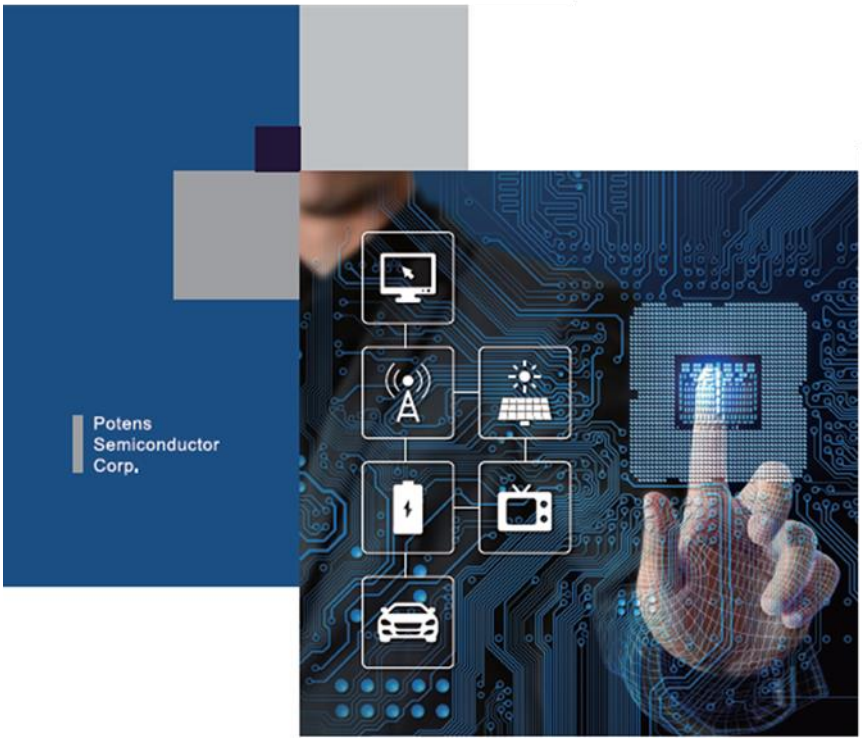
# Application Information

## LED Driver Compatibility with MOSFET




*Enhancing everyday life*

In switching power supply for LED TV drive applications, the gate drive pin with long layout circuit loop of the control IC would be damaged by the negative voltage over the maximum rating. The reason is that the parasitic inductance of the MOSFET lead and PCB circuit trace. Therefore, the reverse recovery time($T_{rr}$) and the reverse recovery charge($Q_{rr}$) of MOSFET's parameters could generate the negative voltage by high current deviation[1]. Fig.1 shows the low-side gate drive circuit loop with parasitic inductance($L_{p1}$), the gate drive voltage ($V_{GS}$), the gate drive resistor voltage ($V_R$), the gate drive current ($I_g$), and gate to source voltage ($V_{gs}$). The voltage ($V_{Lp1}$)of parasitic inductance ($L_{p1}$) can be expressed as

$$V_{Lp1} = L_{p1}\frac{dI_{dr}}{dt} \tag{1}$$

where $I_{dr}$ is the current of body diode. Fig. 2 is the relation between the reverse current of body diode and the voltage of parasitic inductance. In these waveforms, $I_{RM}$ is the maximum reverse current of body diode, $t_{rr\_P}$ is the period of the positive induced voltage and $t_{rr\_N}$ is the period of the negative induced voltage. Therefore, the magnitude of the negative voltage can be derived as

$$V_{Lp1} = -L_{p1}\frac{I_{RM}}{t_{rr\_N}} \tag{2}$$

The relation of the reverse recovery charge, the reverse recovery time and the maximum reverse current is shown as

$$Q_{rr} = \frac{1}{2}I_{RM} \times t_{rr} \tag{3}$$

The duration of the negative voltage means the energy stress on the gate drive pin of the control IC. The more duration the negative voltage sustain, the more the control IC will be damaged. We can drive the negative voltage energy as

$$A = |V_{Lp1}| \times t_{rr\_N} \tag{4}$$

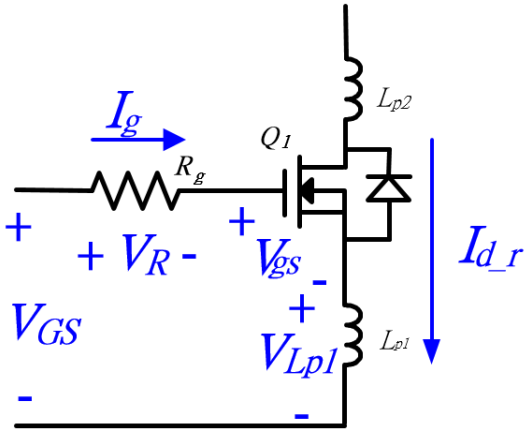



Fig. 1 The low-side gate drive circuit with parasitic inductance.

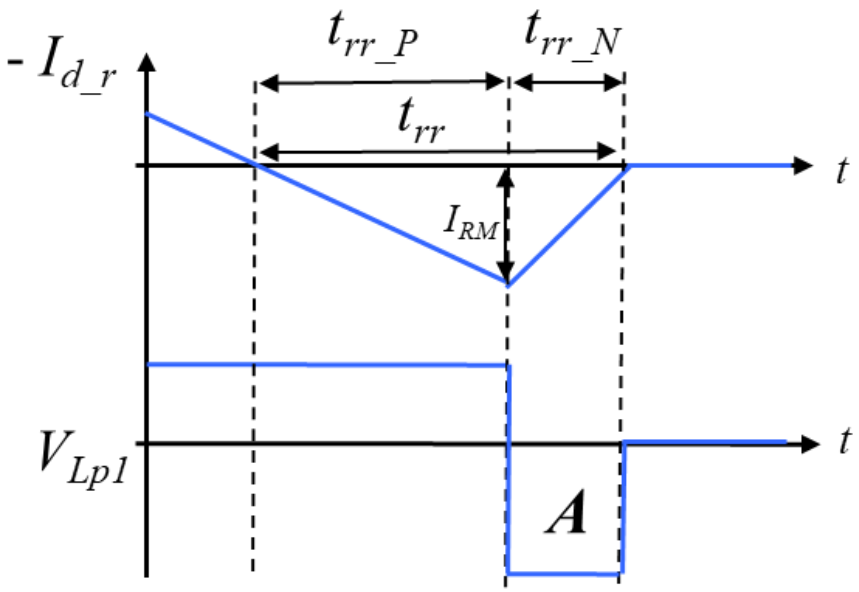



Fig. 2 Relation between the Id current and the voltage

Substitute equation (2) and (3) into (4), we can derive the area of the negative voltage energy as

$$A = 2 \times L_{p1} \times \frac{Q_{rr}}{t_{rr}} \tag{5}$$

The equation (5) means that the energy might damage the IC is related to the ratio of the reverse recovery charge and the reverse recovery time. Fig 3 shows the measurement waveform of the reverse current of super junction MOSFET (PJD11N65N) [2]. The reverse current is about18.05A, the period of the negative induced voltage is 50.3ns and the reverse recovery time is about 254.9ns. For example, there are three different MOSFETs tested and assume that parasitic inductance $L_{pl}$=10nH. The measurement data of these three MOSFETs and the calculation results are shown in Table I.

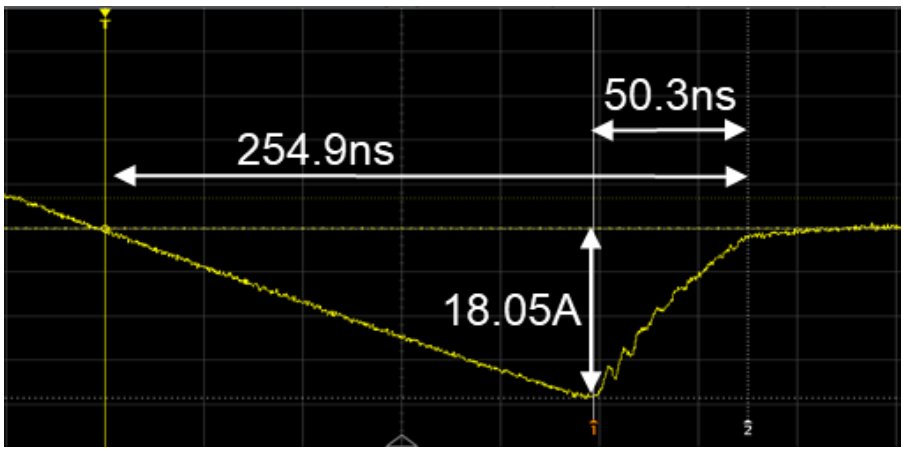



Fig. 3 The measurement of the reverse current

Table I. Relation of MOSFET parameters and negative voltage

| No. | $t_{rr}$ (ns) | $Q_{rr}$ (nC) | $I_{RM}$ (A) | $t_{rr\_N}$ (ns) | $V_{Lp1}$ (V) | $A = V_{Lp1} \times t_{rr\_N}$ (V·ns) | $\frac{Q_{rr}}{t_{rr}}$ |
|---|---|---|---|---|---|---|---|
| Sample 1 | 229.6 | 1946 | 16.95 | 40.45 | -4.19 | 169.5 | 8.5 |
| Sample 2 | 244.1 | 2139 | 17.52 | 58.2 | -3.01 | 175.2 | 8.8 |
| Sample 3 | 254.9 | 2300 | 18.05 | 50.3 | -3.58 | 180.5 | 9 |

From the table I, we could conclude that the sample 3 with ratio of the reverse recovery charge and the reverse recovery time is the highest possibility to damage the gate drive pin of the control IC. There are many methods to eliminate the magnitude of the negative voltage. The simplest method is to increase the gate drive resistor. The gate drive voltage can be derive as

$$V_{GS} = V_{Lp1} + V_R + V_{gs} = L_{p1}\frac{dI_{d\_r}}{dt} + V_{gs} + I_g \times R_g \tag{6}$$

When the gate drive resistor is increased, the magnitude of the negative voltage is decrease as the following relationship:

$$R_g \uparrow \Rightarrow |V_{GS}| \downarrow \tag{7}$$

The smaller the negative voltage is, the smaller the energy is. Therefore, the possibility for IC damaged is being smaller.

Reference


[1] C. G. Chen, S. H. Lee, C. M. Yu, W. N. Huang 1, J. S. Lee, H. C. Meng and T. M. Lai, "Negative Voltage Analysis Model for Evaluation on Control IC Driving of MOSFET Application," in *4th International Conference on Microelectronic Devices and Technologies (MicDAT '2022)*, Corfu, Greece, 21-23 Sep. 2022, pp. 5-8.

[2] Potens Semiconductor, "Super Junction N-channel MOSFET," PJD11N65N datasheet. https://www.potens-semi.com/upload/product/PJD11N65N.pdf.